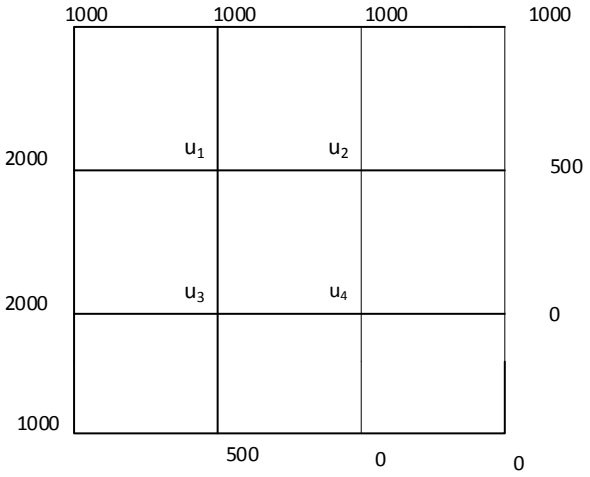
BRACH: VLSI DESIGN

IES COLLEGE OF TECHNOLOGY, BHOPAL
M.E./ M.Tech.(1th SEM) Assignment -1
Advanced Mathematics (MEVD-101)

Date of Assignment: 18/09/14 **Date of Submission:17/10/2014**

Note:1.Question should be written in plain A-4 Size Paper.
2.Minimum 300 Word Limit for each Question.
3.Assignment should be submit in stick file.

Q.1	Using method of separation of variables, solve: $$\frac{\partial u}{\partial x} = 2\frac{\partial u}{\partial x} + u$$ where, $u(x,0) = 6e^{-3x}$	Mar., 2010
Q.2	Define binomial distribution. The probability the pen manufactured by a company will be defective is $\frac{1}{10}$. If 12 such pens are manufactured, find the probability that a. Exactly two will be defective b. At least two will be defective c. None will be defective.	Mar. ,2010
Q.3	Find the solution of two- dimensional heat equation.	June, 2011
Q.4	Solve the elliptic equation $u_{xx} + u_{yy} = 0$ for the following square mesh with boundary values as shown:  	Dec., 2010
Q.5	Find the Fourier transform of : $$f(x) = \begin{cases} 1 \; for \; \lvert x \rvert < 1 \\ 0 \; for \; \lvert x \rvert > 1 \end{cases}$$ Hence evaluate: $$\int_0^\infty \frac{\sin x}{x} dx$$	Mar., 2010

IES COLLEGE OF TECHNOLOGY, BHOPAL

M.Tech Assignment-1(Unit 1 & 2)

Subject-MEVD-102 VLSI Design

Date of Assignment: 18/09/14 **Date of Submission:17/10/2014**

Note: 1.Minimum 300 Word Limit for each Question.

2.Diagram should be neat and clean.

Q.1	Describe different parasitic effect in integrated circuits? (2012)
Q.2	Explain CMOS Process. And also explain n & p channel MOSFET. (2011)
Q.3	Difference b/w Bipolar and CMOS Technologies. And define threshold voltage in CMOS.(2013) (300 words)
Q.4	Explain device modeling, DC model, Diode model, BJT model. (2011)
Q.5	What is circuit simulation? Explain Body Effect, Noise Margin.(2012)

IES COLLEGE OF TECHNOLOGY, BHOPAL

M.Tech Assignment-1(Unit 1 & 2)

Subject-MEVD-103

Advanced Logic Design Design

Date of Assignment: 18/09/14 **Date of Submission:17/10/2014**

Note: 1.Minimum 300 Word Limit for each Question.

2.Diagram should be neat and clean.

Q.1	Describe various verilog data types &operators (2012)
Q.2	Design CMOS NAND gate and discuss its working principle . (2012)
Q.3	Explain briefly about the working of programmable logic device .CMOS.(2012)
Q.4	Simplify the expiration Y =∑m(3,4,5,7,9,13,14,15) using K-map method and then implement the function using NAND gates.(2012)
Q.5	Write verilog module for one bit full adder using built in verilog gates.2011

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M.Tech Assignment-1(Unit 1 & 2)

Subject- MEVD-104 DSP

Date of Assignment: 18/09/14 **Date of Submission:17/10/2014**

Note: 1.Minimum 300 Word Limit for each Question.

2.Diagram should be neat and clean.

Q.1	Q1 Explain recursive and non recursive system.(2011)
Q.2	Q2 Define R.O.C and also explain its properties for the z- Transform .(2012)
Q.3	Q3 Use convolution to find X(n) if is given by $X(Z)=1/(1-1/2z^{-1})(1+1/4^{z-1})$ (2013)
Q.4	Q4 Find the two sided Z- transform of $x(n) = (1/3)^n$ n≥0 (-2)n n≤-1 (2012)
Q.5	Q 5 Explain Matched Z-transform. (2011)

IES COLLEGE OF TECHNOLOGY, BHOPAL

M.Tech Assignment-1(Unit 1 & 2)

Subject- MEVD 105 Embedded System Design

: **Date of Assignment: 18/09/14** **Date of Submission:17/10/2014**

Note: 1.Minimum 300 Word Limit for each Question.

2.Diagram should be neat and clean.

Q.1	Explain Introduction to Embedded system, And explain basic concept of Embedded System Project Management process.(2011)
Q.2	Explain Microcontrollers and DSP Processors? (2012)
Q.3	Explain Serial Communication Protocols, Parallel Communication Protocols.(2013)
Q.4	Explain ROM, EPROM, EEPROM, FLASH, RAM, SRAM, DRAM? (2011)
Q.5	Describe the role of embedded processor in vlsi circuits? (2012)