Solution of

Basic Electrical and Electronics Engineering – BE -104

RGPV End Semester Examination – June 2014

Ans 1 (a) :-

Voltage Source :-

An ideal / independent voltage source is defined as the energy source which gives constant voltage across its terminals irrespective of the current drawn from/through its terminals. However, a practical voltage source has small internal resistance and it is represented in series with voltage source and denoted as R_i, Because of internal resis-tance R_i, the terminal voltage decreases with increase in current

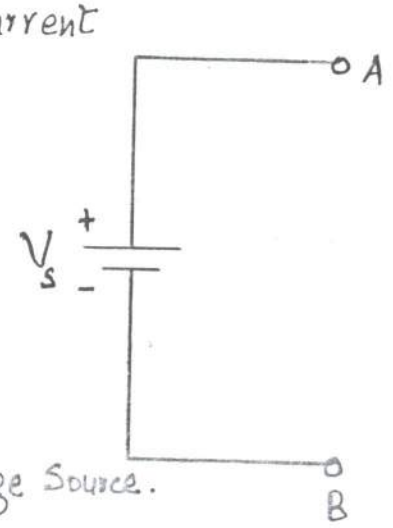


Fig:- Ideal Voltage Source.

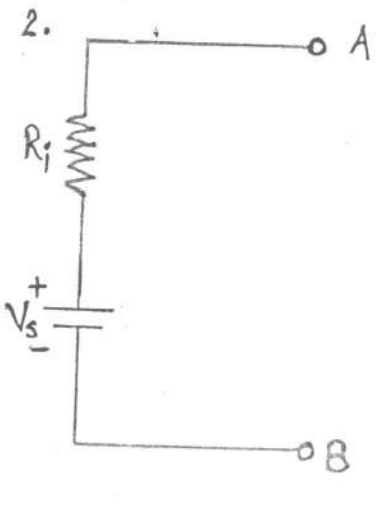


Fig:- Practical Voltage Source.

Current Source :-

An ideal current source is the source which gives constant current at its terminals irrespective of the voltage appearing across its terminals. However, a practical current

source has high internal resistance and it is represented in parallel with current source and represented as R_{sh} or R_i.

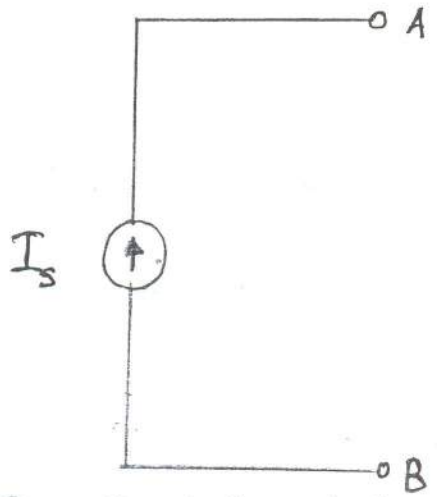


Fig:- Ideal Current Source

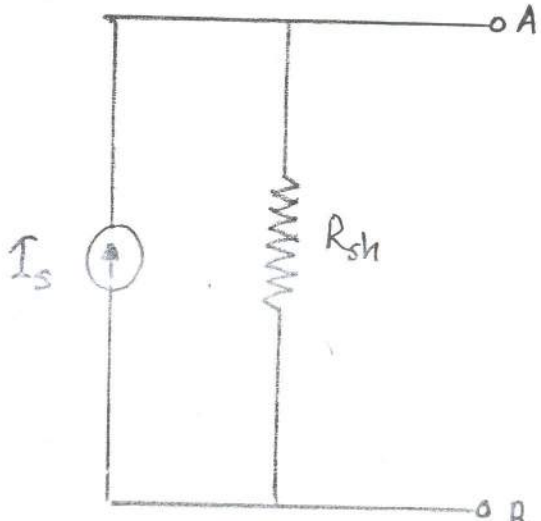


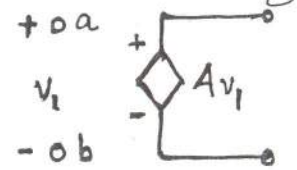
Fig: Practical Current Source.

Ans 1 (b) :-

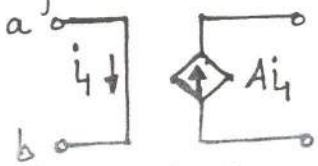
Dependent Source :-

A dependent source is one which depends on some other quantity defined elsewhere in the circuit which may be either voltage or current. Dependent sources are classified as :-

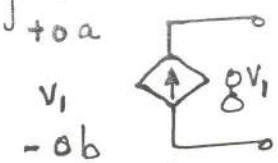
1. Voltage Dependent Voltage Source:-



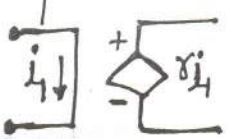
2. Current Dependtdent Current Source:-



3. Current Dependent Voltage Source:-



4. Voltage Dependent Current Source :-



Dependent Sources are encountered in modelling of electronic devices.

Independent Source :-

A source is said to be independent when it does not depend on any other quantity in the circuit. An independent source can be ideal voltage source or ideal current source or both. Independent sources actually exist as physical entities such as an accumulator; a dc generator and an alternator.

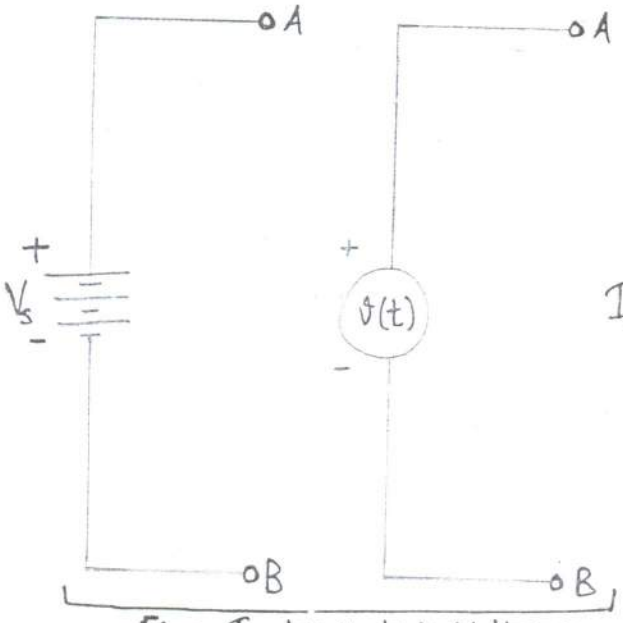


Fig:- Independent Voltage Sources

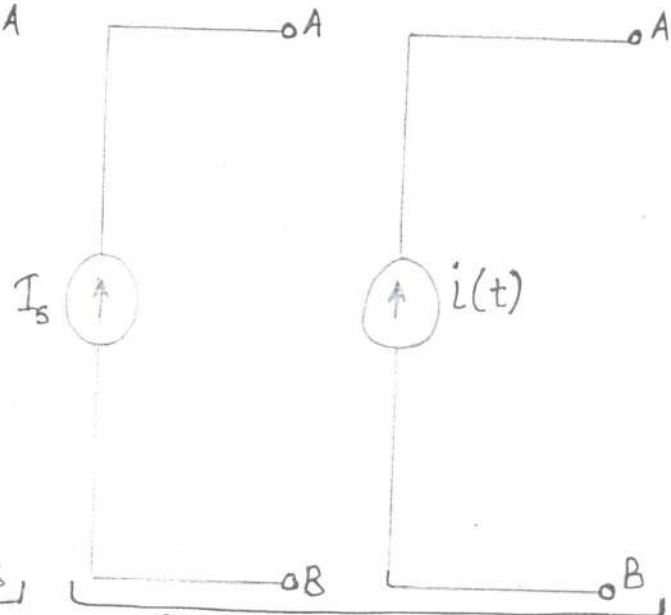


Fig:- Independent Current Sources

Ans 1 (c):-

Given :- $P = 2000W$

$\cos\theta = .8$

$V = 230$ Volts.

Now, Load current is determined as :-

$$I = \frac{P}{V\cos\theta} = \frac{2000}{230 \times .8}$$

$$= 10.86 \text{ Amp's}$$

Active Power; P already given = 2kW
= 2000W. Ans.

Reactive Power; $Q = VI\sin\theta$ VAR

$= 230 \times 10.86 \times .6$ VAR.

$= 1498.68$ VAR Ans

Apparent Power; $S = V \times I$ VA

$= 230 \times 10.86$

$= 2497.8$ VA. Ans

Ans 1(d):-

Let's consider an inductive load and let the instantaneou voltage be

$$v = V_{max} \sin\omega t \quad — (1)$$

Then the current drawn from the supply for load is

$$i = I_{max} \sin(\omega t - \theta) \quad — (2)$$

where, θ is the angle by which the current lags the voltage.

The instantaneous power is defined as :-

$$p = v \times i$$

$$= V_{max} \sin\omega t \times I_{max} \sin(\omega t - \theta)$$

$$= V_{max} I_{max} \sin\omega t \sin(\omega t - \theta) \quad — (3)$$

Using trigonometric identities, we have

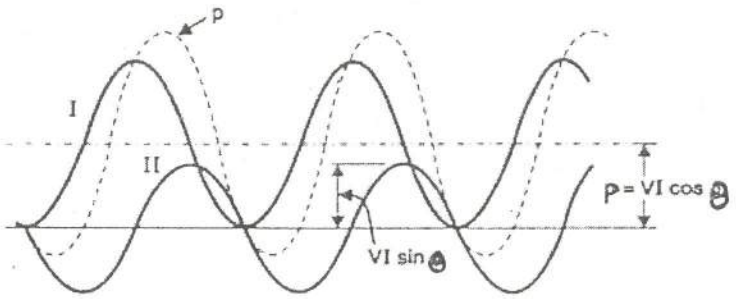
$$p = \underbrace{VI\cos\theta(1-\cos 2\omega t)}_{\text{I}} - \underbrace{VI\sin\theta\sin 2\omega t}_{\text{II}} \quad \text{— (4)}$$

So, the instantaneous power is decomposed into two components. We are interested to discuss second (II) component

The component marked II contains the term $\sin\theta$ which is negative for capacitive load and positive for inductive load. This component pulsates at twice the supply frequency and has zero as its average value. This component is known as <u>reactive power</u> as it travels back and forth on the line without doing any useful work.

Alternatively speaking, the quadrature component of current $I\sin\theta$ feeds only oscillating power (frequency 2ω) to the load with zero average value. It is the reactive power.

$$\boxed{Q = VI\sin\theta \quad (VAR)} \quad \text{— (5)}$$



Active, reactive and total power in a single phase circuit.

The reactive power is exchanged by different parts of the network - capacitors and reactors - permanently, but is never consumed or produced.

Also, $\boxed{Q = I^2X_L \quad VAR}$

OR

Ans 1 (d):-

A three phase balanced supply consists of three phase voltages equal in magnitude and phase displaced by 120° from one another. The instantaneous values of three phase voltages can be expressed as:-

$$v_{aa'} = V_{max} \sin \omega t$$

$$v_{bb'} = V_{max} \sin(\omega t - 120°)$$

$$v_{cc'} = V_{max} \sin(\omega t - 240°).$$

A three phase supply will be unbalanced when either of the three phase voltages are unequal in magnitude or the phase angle between three phases is not equal to 120°.

Impact of unbalanced load on power supply:-

(i) When the three phase load is unbalanced in nature, then the neutral wire carries current as a consequence of which voltage drop takes place in neutral wire. Due to neutral wire drop, the neutral-pin at the consumer locations will differ in potential from transformer neutral point. This difference will be more if neutral is carrying heavy currents. This problem of neutral-earth voltage difference is called neutral-shift problem. Electronic equipment in general, and, computing equipment in particular, are sensitive to this neutral-shift voltage and often malfunction when it exceeds certain pre-specified levels.

(2) The negative sequence current drawn by unbalanced load is a wasteful current that ties up equipment capacity and increases system losses without carrying productive power. Such currents are unproductive in effect and detrimental to power supply.

Ans 2(a) :-

Consider an ideal transformer being connected to load.

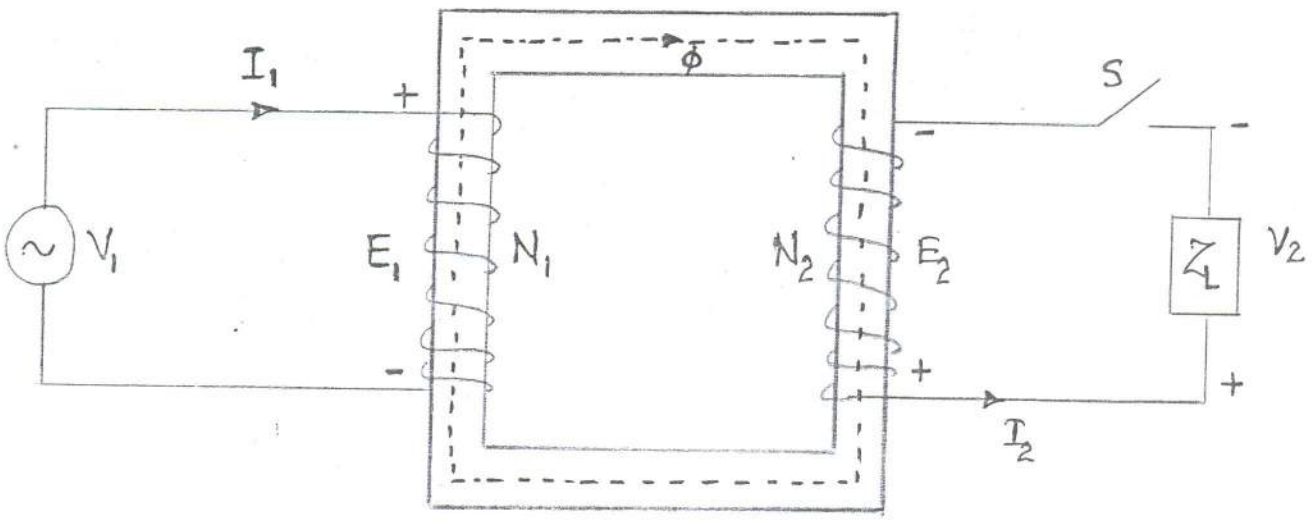
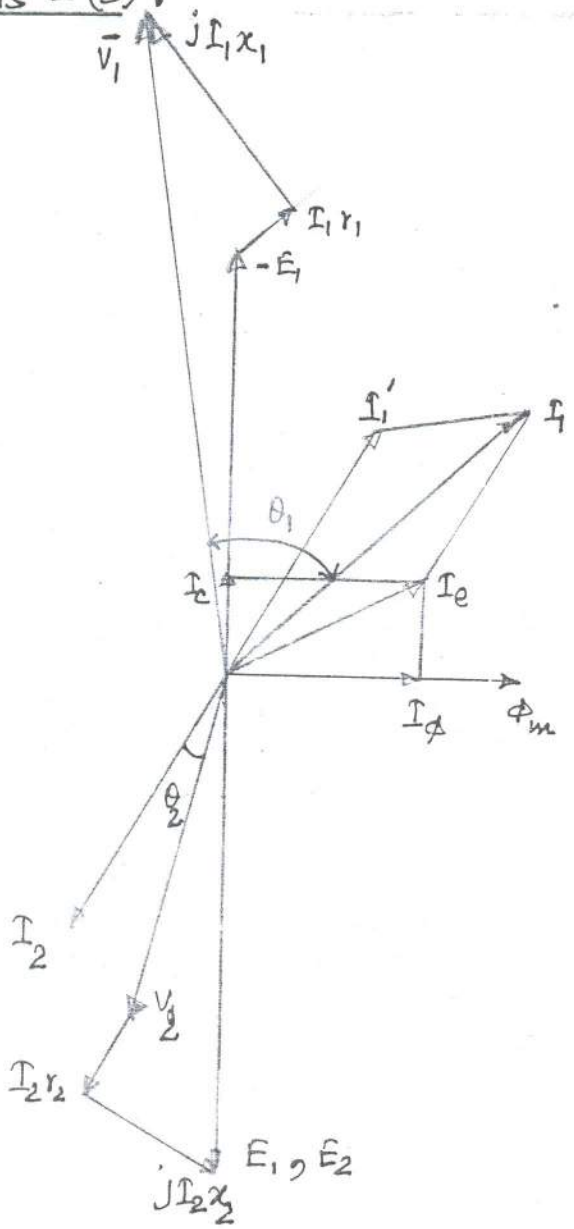


Fig:- Ideal transformer on load

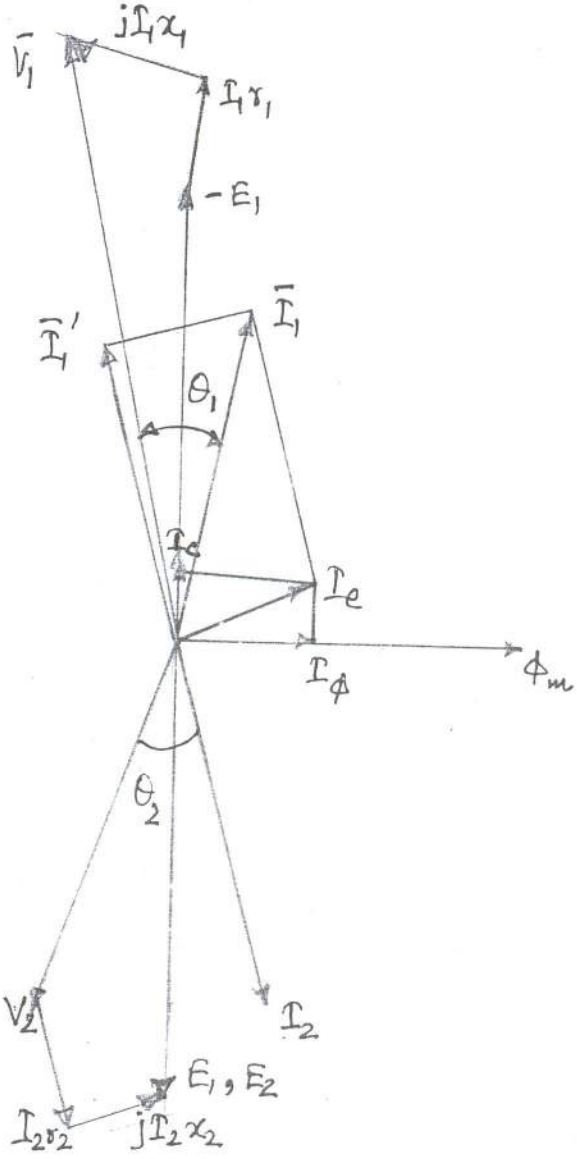
Now let the switch S is closed; as a result of which a load impedance Z_L gets connected across the secondary terminals. Since the secondary feeds a sinusoidal current of instantaneous value i_2 to the load; the secondary creates mmf $F_2 = i_2 N_2$ being opposite to mutual flux ϕ in the core as per Lenz's Law. However, the mutual flux ϕ cannot change as otherwise (V_1, e_1) balance will be disturbed (this balance must always be hold as winding has zero leakage and resistance). The result is that the primary draws a current i_1 from the source so as to create mmf $F_1 = i_1 N_1$ which at all time cancels out the load current mmf $N_2 i_2$ so that mutual flux ϕ is maintained constant independent of the load current flow.

Even in practical transformers also, the mutual does not change appreciably from no load to full load.

Ans 2(b) :-



(1) Phasor diagram for inductive load.



(2) Phasor diagram for Capacitive load.

It is easily understood from above phasor diagrams that in case of capacitive load (1) Load current I_2 leads the secondary terminal voltage by θ_2 (2) primary power factor $\cos\theta_1$ is high as compared to that in case of inductive load.

Ans 2(c):-

The equivalent circuit for any electrical engineering device can be drawn if the equations describing its behaviour are known. If any electrical device is to be analysed and investigated further for any suitable modifications, its appropriate equivalent circuit is necessary. An equivalent circuit can easily be studied and analysed by the direct application of electric circuit theory.

The equivalent circuit of transformer should be used only when the exciting current is a large percentage of the rated current ie. in audio-frequency transformers used in electronic circuits, in transformers used for relaying and measurement purpose. Further, the equivalent circuit of transformer is also used in those situations, when a large power system is studied.

Ans 2(d):-

$$S = 500\ KVA$$
$$= 500 \times 10^3\ VA$$

$$\eta = \frac{m S \cos\theta_2}{m S \cos\theta_2 + P_i + m^2 P_{cfL}}$$

(i)

→ At full load ie $m = 1$

$$.9 = \frac{1 \times 500 \times 10^3 \times 1}{1 \times 500 \times 10^3 \times 1 + P_i + P_{cfL}}$$

$$.9 = \frac{500 \times 10^3}{500000 + P_i + P_{cfL}} \quad - (1)$$

At 70% of full load ($m = .7$)

$$.9 = \frac{.7 \times 500 \times 10^3 \times 1}{.7 \times 500 \times 10^3 \times 1 + P_i + (.7)^2 P_{cfL}} \quad -(2)$$

from equation (1) and (2)

$$450000 + .9P_i + .9P_{cfL} = 500000$$

or $$P_i + P_{cfL} = 55556 \quad -(3)$$

and $$315000 + .9P_i + .44P_{cfl} = 350000$$

$$.9P_i + .44P_{cfl} = 35000 \quad -(4)$$

Equating and solving eq (3) and (4)

$$.9(55556 - P_{cfl}) + .44P_{cfl} = 35000$$

$$50000 - .9P_{cfl} + .44P_{cfl} = 35000$$

or $$15000 = .46P_{cfL}$$

or $$P_{cfL} = 32609.5 \text{ Watts}$$

Now $$P_i = 55556 - 32609.5$$

$$= 22946.5 \text{ Watts}$$

So, $P_{cfL} = 32609.5$ W
and $P_i = 22946.5$ W

Ans.

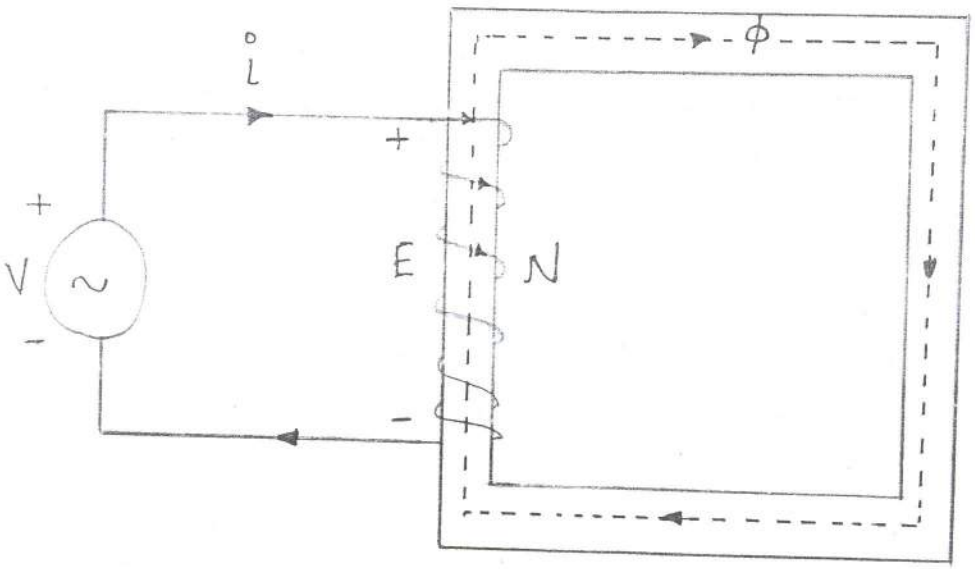
(ii) $$\eta_{.8FL} = \frac{.8 \times 500 \times 10^3 \times 1}{.8 \times 500 \times 1000 \times 1 + 22946.5 + (.8)^2 32609.5}$$

$$\eta_{80\%FL} = 90.12\ \%$$ Answer

OR

Ans 2(d) :-

Consider an N-turn iron-core coil with ac excitation. The coil is assumed to be ideal with zero resistance. The induced emf in the coil must be simusoidal for it to balance the ac applied voltage. This constrains the flux in the core to be simusoidal.



Let $\phi = \phi_{max} \sin \omega t$ — (1)

where

ϕ_{max} = maximum core flux

$\omega = 2\pi f$ rad/sec.

f = frequency of excitation in Hz.

The emf induced in the coil as per Faraday's law

$$v = e = N\frac{d\phi}{dt}$$

$$= N\frac{d}{dt}\phi_{max}\sin\omega t$$

$$e = N\phi_{max}\omega\cos\omega t$$

$$e = E_{max}\cos\omega t \quad \text{—— (2)}$$

where

$$E_{max} = N\phi_{max}\omega.$$

Now, RMS value of induced emf

$$E = \frac{E_{max}}{\sqrt{2}} = \frac{N\phi_{max}2\pi f}{\sqrt{2}}$$

or $$E = \sqrt{2}\pi f N\phi_{max}$$

or $$V = E = 4.44 f N\phi_{max}$$

or, $$\boxed{\phi_{max} = \frac{V}{4.44 f N}} \quad \text{—— (3).}$$

So, Maximum value of the core flux or flux density is dictated by the voltage applied to the coil and is independent of core reluctance.

Ans 3 (a) :- A three phase rotating machine (both induction machine and synchronous machine) mainly consists two constructional parts :-

1. Stator
2. Rotor.

The constructional features of stator are identical for both induction machine and synchronous machine.

Stator is the stationary part of the machine- and consists of stator frame, stator core, polyphase distributed winding, two end covers, bearings etc. The construc-tional feature of stator is shown as follows :-

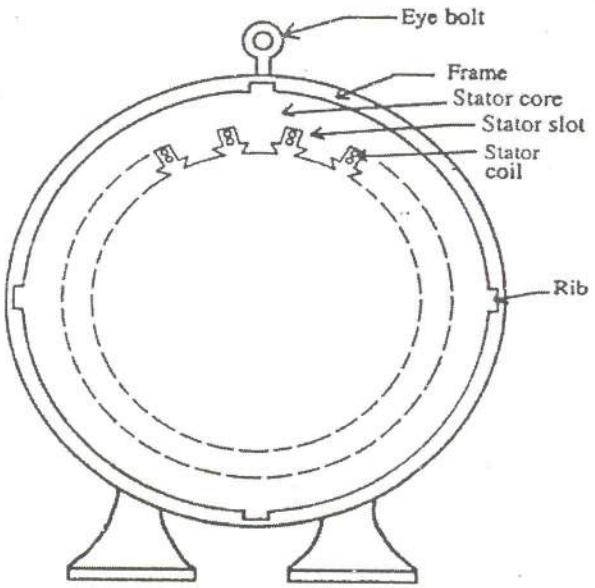


Fig :- Stator Construction

The rotor is the rotating part of three phase machine The induction machine has two types of rotors :-

(1) the squirrel cage rotor and

(2) wound rotor.

The constructional feature of both the types of rotors is shown below :-

1.

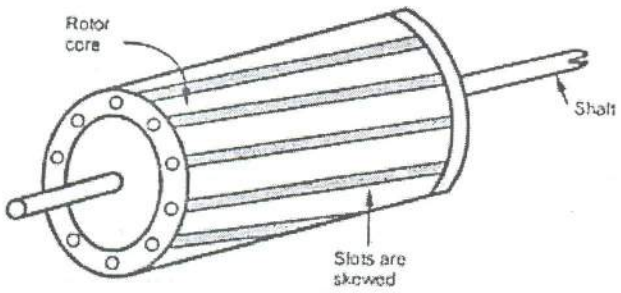


Fig:- Squirrel Cage Rotor

2.

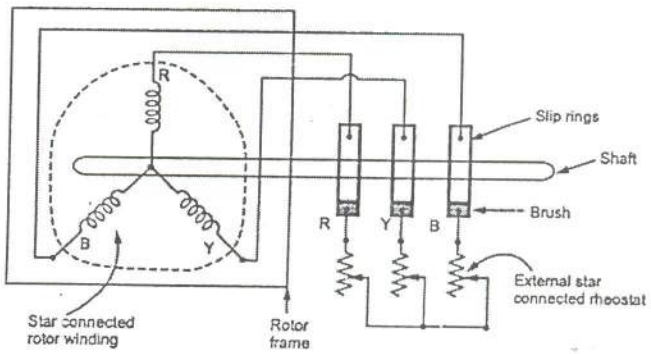


Fig:- Wound/Cylindrical Rotor.

Similarly, a three phase synchronous machine also has two types of rotors shown below:-

(1) Salient Pole Type (2) Non-salient pole type or smooth cylindrical type

1.

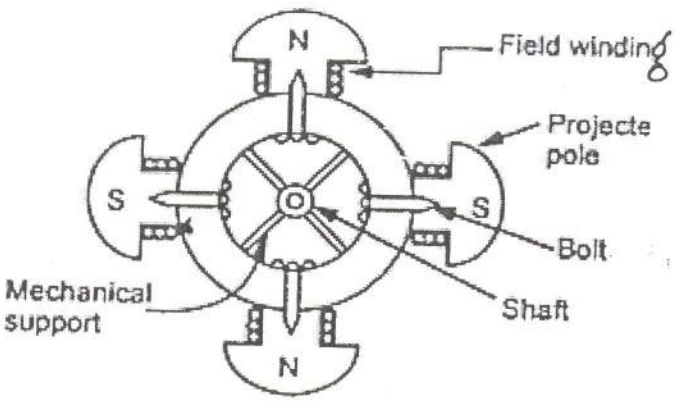


Fig:- Salient Pole Rotor

2.

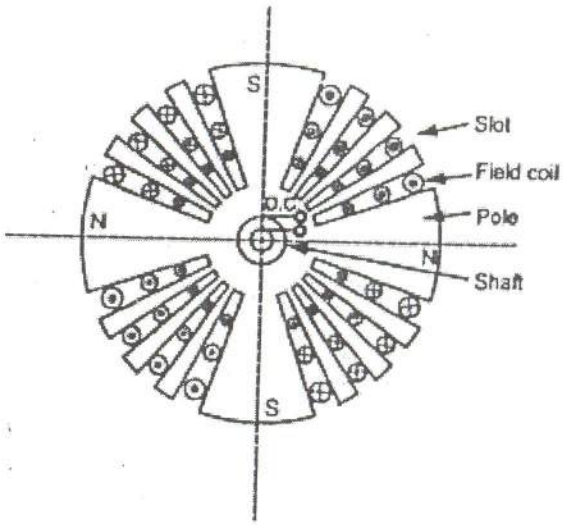


Fig:- Non Salient Pole Rotor.

Ans 3(b) :-

When a balanced three phase voltages at line frequency f_1 are supplied to the stator winding, a rotating magnetic field is produced. This rotating magnetic flux cuts both the stator and stationary rotor conductors at synchronous speed, consequently emfs of line frequency f_1 are induced in them.

The coil induced emf per phase is given by

$$e_1 = -\frac{d\lambda}{dt}$$

$$= -\frac{d}{dt}(N_1\phi\cos\omega t)$$

$$e_1 = \omega N_1\phi \sin\omega t$$

or $$e = E_{1max}\sin\omega t$$

where $E_{1max} = \omega N_1\phi$

ϕ = total useful flux per pole (Wb).

Now; rms value of emf induced in the coil is given by:

$$E_1 = \frac{E_{1max}}{\sqrt{2}} = \frac{2\pi f_1 N_1\phi}{\sqrt{2}}$$

$$= 4.44 \times f_1 \times N_1 \times \phi$$

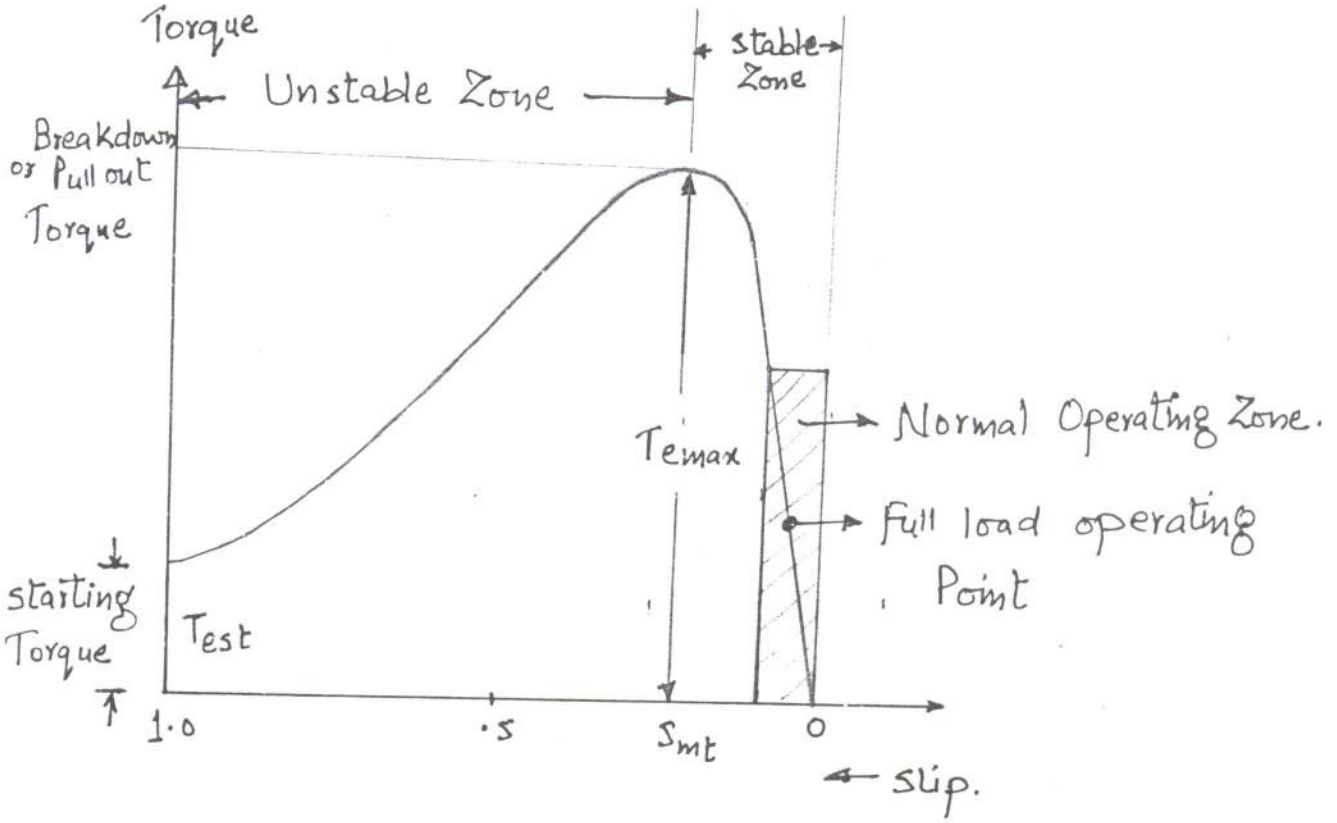
OR $$\boxed{E_1 = 4.44 \times f_1 \times k_{w1} \times N_1 \times \phi}$$

where E_1 = Per phase value of emf E_1 induced in stator winding.
N_1 = stator series turns per phase
k_{w1} = stator winding factor.

Similarly, per phase emf E_2 induced in standstill rotor winding:

$$E_2 = 4.44 \times f_1 \times k_{w2} \times N_2 \times \phi$$

Ans 3 (c) :- The torque-slip characteristics of an induction motor is shown as follows:-



Condition for Maximum Torque :-

The value of torque when motor is running is given by

$$T_d = \frac{k s R_2 E_{20}^2}{R_2^2 + (s X_{20})^2} \quad N-m \quad -(1).$$

where, $k = \frac{3}{2\pi n_s}$

E_{20} = emf induced in the per phase rotor winding at still.

s = motor slip.

If the impedance of the stator winding is assumed to be negligible, then for given supply voltage V_1, E_{20} remain constant.

Let $k E_{20}^2 = k_1$ (a constant)

$$\therefore \quad T_d = \frac{k_1 R_2}{\frac{R_2^2}{s} + s X_{20}^2}$$

$$= \frac{k_1 R_2}{\left(\frac{R_2}{\sqrt{s}} - X_{20}\sqrt{s}\right)^2 + 2 R_2 X_{20}} \qquad \text{— (2)}$$

The develop torque T_d will be maximum when RHS of eq(2) is maximum which is possible when

$$\frac{R_2}{\sqrt{s}} - X_{20}\sqrt{s} = 0$$

$$\text{or} \quad R_2 = s X_{20}$$

$$\text{or} \quad \boxed{R_2 = X_{2s}} \qquad \text{—— (3)}$$

i.e. the developed torque is maximum when rotor resistance per phase is equal to rotor reactance per phase under running conditions.

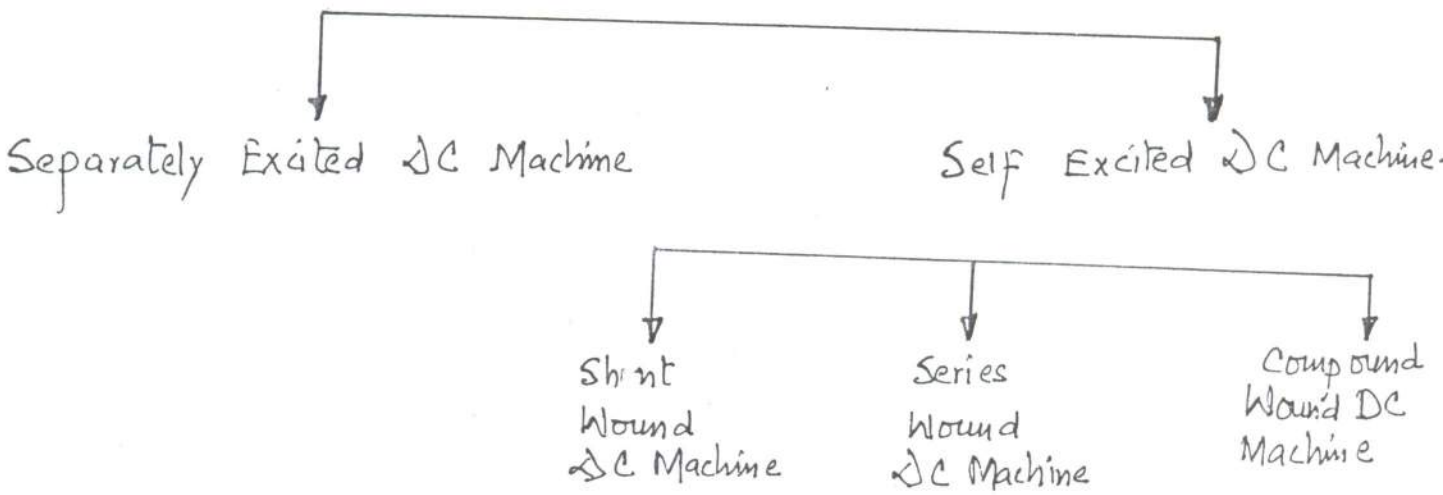
Ans 3 (d) :-

D.C. Machines are classified on the basis of how the required excitation or magnetic flux is produced. There are, in general, two methods of exciting the

field windings of dc machines:

(a) Separate excitation and
(b) Self excitation.

So, DC Machines are broadly classified as:-



1. Separately Exited DC Machine :-

As the name implies, the field coils are energised by a separate dc source. The voltage of the external dc source has no relation with the armature voltage i.e. the field winding energised from a separate supply can be designed for any convenient voltage.

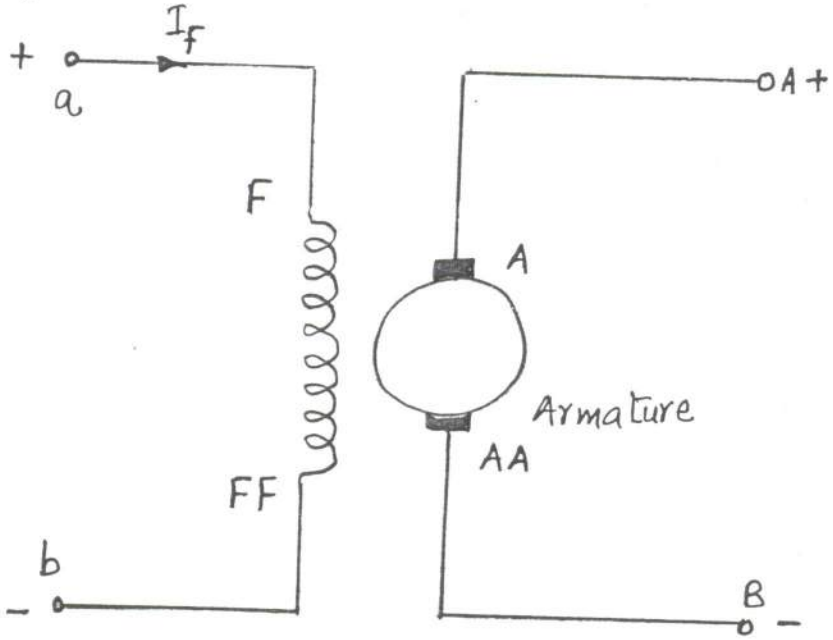


Fig:- Separately Exited DC Machine.

2. Self Excited DC Machine :-

When the field winding is excited by its own armature, the machine is said to be self excited. A self excited dc machine can be subdivided as follows :-

Shund Wound/Excited DC Machine :-

The field winding consists of large number of turns of fine wire and is connected in parallel with the armature. The shunt field coil is called as voltage-operated field.

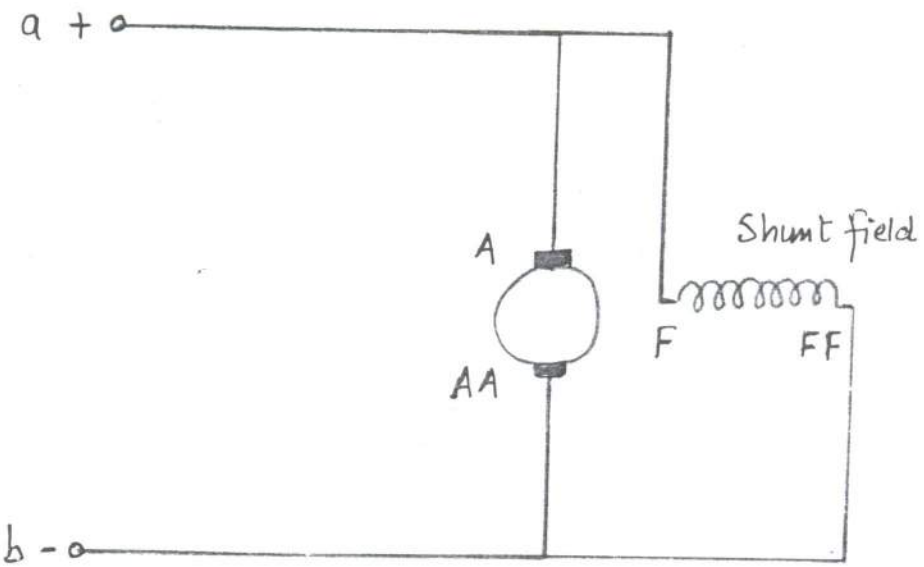


Fig:-
Shunt Excited
DC Machine

Series Wound/Excited DC Machine :-

The field winding consists of a few turns of thick wire and is connected in serie with the armature. A series field may be called as current operated field.

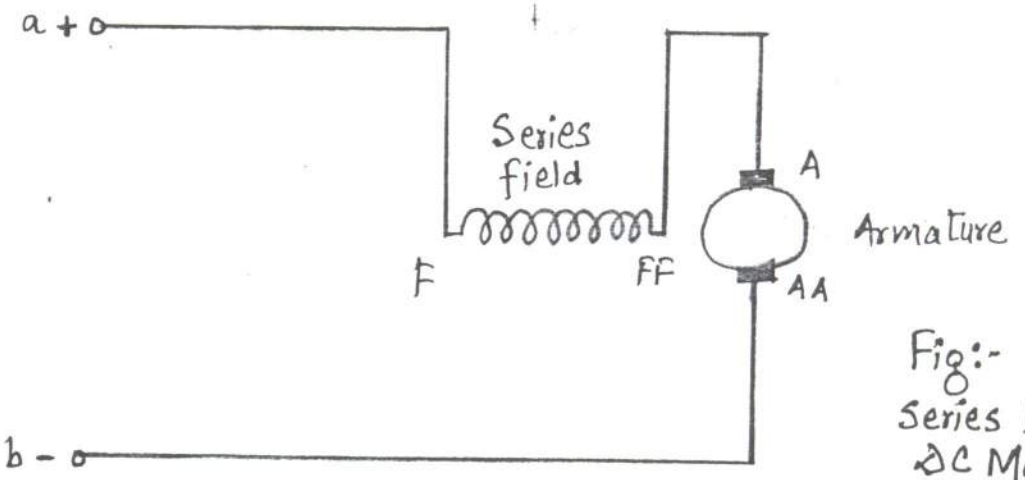


Fig:-
Series Excited
DC Machine.

Compound Wound/Excited DC Machine :-

A compound excitation involves both the series excited winding and the shunt excited winding. from the view-point of connections, a dc Compound machine may short-shunt connection or long-shunt connection. In short-shunt connection, the shunt field is connected across the armature terminals, whereas, in the long-shunt connection, the shunt field winding is connected across the machine or line terminals.

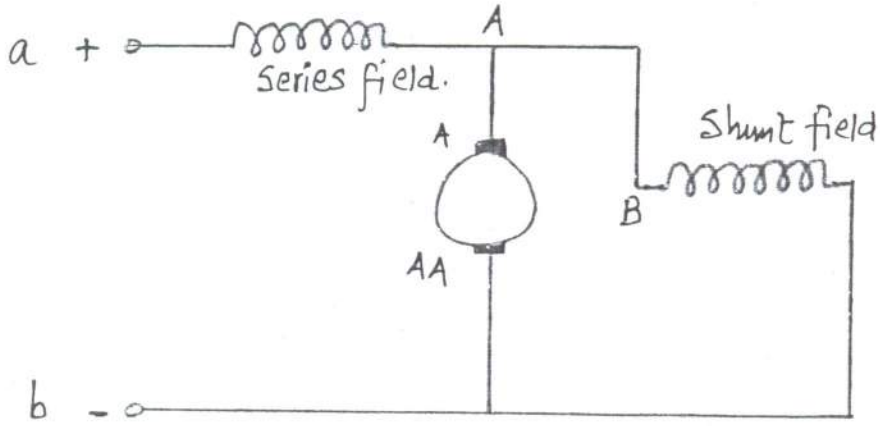


Fig:- Short shunt DC Machine

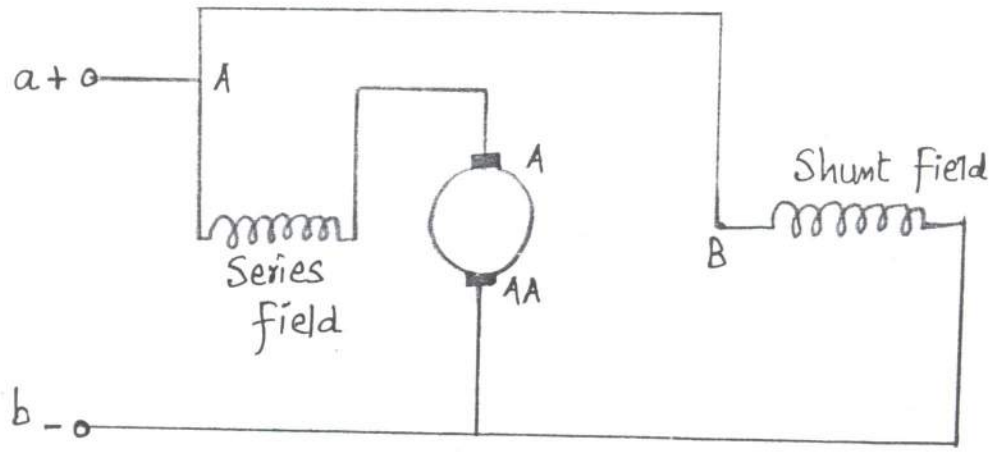


Fig:- Long Shunt DC Machine.

OR

Ans 3 (d)

As per the conditions mentioned in the question, we have to consider two cases i.e. Initial condition and final condition.

Initial Condition

$E_1 = V - I_{a_1}(R_a + R_{se})$

$= 230 - 110(.12 + .03)$

$= 230 - 16.5$

$= 213.5$ volts.

Final Condition

$E_2 = V - I_{a2}(R_a + R_{se})$

$E_2 = 230 - 50(.03 + .12)$

$= 230 - 7.5$

$= 222.5$ volts.

Now, in case of dc motors

$$E_b \propto \phi N$$

or $$\frac{E_1}{E_2} = \frac{N_1}{N_2} \times \frac{\phi_1}{\phi_2}$$

$$\frac{213.5}{222.5} = \frac{600}{N_2} \times \frac{24 \times 10^{-3}}{16 \times 10^{-3}}$$

or $$N_2 = \frac{600 \times 24 \times 10^{-3} \times 222.5}{213.5 \times 16 \times 10^{-3}}$$

$$\boxed{N_2 = 937.93 \text{ rpm}}$$ Ans.

Ans 4 (a) :-

The different number systems used in digital electronics are :-

1. Decimal Number System :-
   * The decimal numerals are the familiar zero through nine (0, 1, 2, 3, 4, 5, 6, 7, 8, 9)
   * The decimal system has a base or radix of 10.

2. Binary Number System :-
   * The binary numerals used in the binary number system are 0 and 1.
   * The binary number system has a base or radix of 2.

3. Octal Number System :-
   * The numbers used in Octal number system are 0, 1, 2, 3, 4, 5, 6, 7
   * The octal number system has a base or radix of 8

4. Hexadecimal Number System :-
   * The hexadecimal numerals are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F.
   * The hexadecimal number system has a base or radix of 16.

Floating Point Numbers :-

Floating Point Number consists of two parts. The first part of the number is a signed fixed point number, which is termed as mantissa, and the second part specifies the decimal or binary point position and is termed as exponent. The mantissa can be an integer or a fraction.

A decimal +12.34 in a typical floating point notation is expressed as :- $\cdot 1234 \times 10^2$

Ans 4 (b) :-

De Morgan's first theorem is stated as follows:-

→ "The complement of a product of variables is equal to the sum of complements of the variables"

$$\text{i.e.} \quad \overline{X.Y} = \bar{X} + \bar{Y}$$

De Morgan's second theorem is stated as follows:-

→ "The complement of a sum of variables is equal to the product of complements of the variables".

$$\overline{X+Y} = \bar{X}.\bar{Y}$$

eg:- (a) $\overline{(\overline{X+Y}) + \bar{Z}}$

$= \overline{\overline{(X+Y)}}\,\overline{\bar{Z}}$ (using De Morgan's second theorem).

$= (X+Y)Z$

(b) $\overline{XYZ} = \bar{X} + \bar{Y} + Z$ (using De Morgan's first theorem).

(c) $(\bar{X}Y)\bar{Z} + \bar{X}(\overline{YZ}) = (\bar{X}+\bar{Y})\bar{Z} + \bar{X}(\bar{Y}+\bar{Z})$

Ans 4(c):- The J-K flip flop is a versatile and is widely used type of flip-flop. A simplified Logic diagram for a positive edge-triggered J-K flip flop is shown as follows :-

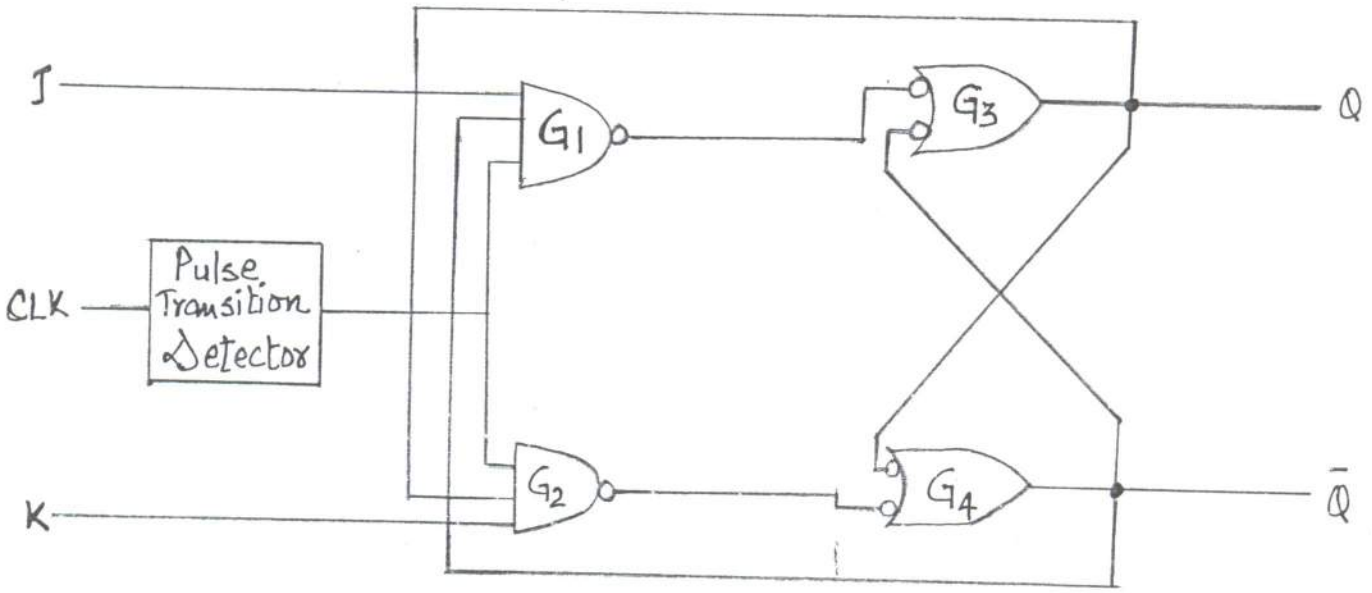


Fig:- Logic Diagram of J-K flip flop.

The operation of the edge-triggered flip flop or J-K flip flop is summarised in truth table given in table below. Notice that there is no invalid states as there is with an S-R flip-flop. The truth table for a negative edge-triggered device is identical except that it is triggered on the falling edge of the clock pulse.

TRUTH TABLE

INPUTS			OUTPUTS		
J	K	CLK	Q	$\bar{Q}$	Comment
0	0	↑	Q_0	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	Q_0	Toggle

↑ = clock transition Low to High

Q_0 = Output level prior to clock transition.

Ans 4(d) :- A **half adder** is the simplest combinational circuit which performs the arithmetic addition of two binary digits. It accepts two binary digits on its inputs and produces two binary digits on its outputs - a Sum bit and a Carry bit. The truth table of half adder is shown as follows :-

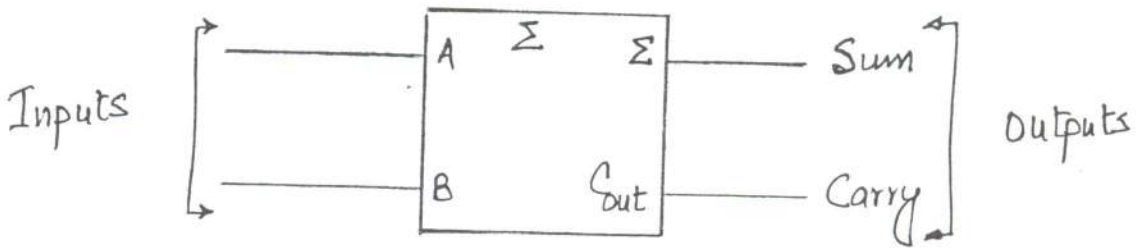


Fig:- Logic Symbol.

Truth Table for Half Adder

A	B	Cout	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

A and B = input variables (operands).

from the truth table, it can understand that the Sum output is 1 when either of the inputs (A or B) is 1, and Carry output is 1 when both the inputs (A and B) are 1.

The logic expression for the Sum output can be written as Sum of Product expression by summing up the input combination for which the sum is equal to 1.

In the truth table; the sum output is 1 when AB = 01 and AB = 10. So, the expression for sum is

$$S = \bar{A}B + A\bar{B} \quad \text{——— (1)}$$

and can be simplified as

$$\boxed{S = A \oplus B} \quad \text{——— (2)}$$

The logic expression for Carry output can be expressed as a Sum of Product expression by summing up the input combinations for which carry is equal to 1. In the truth table, the carry is 1 when AB = 11. So,

$$\boxed{C = AB} \quad \text{——— (3).}$$

The logic diagrams for Half adder using Ex-OR and AND gates is shown as follows:-

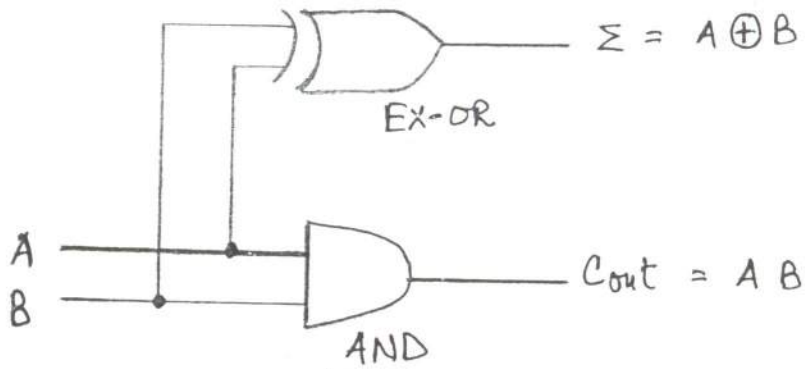


Fig:- Half Adder Logic Diagram.

A **full adder** is a combinational circuit that performs the arithmetic sum of three input bits and produces a sum and a carry. The full adder accepts two input bits and an input carry and generates a sum output and an output carry.

A logic symbol for a full adder is shown below.

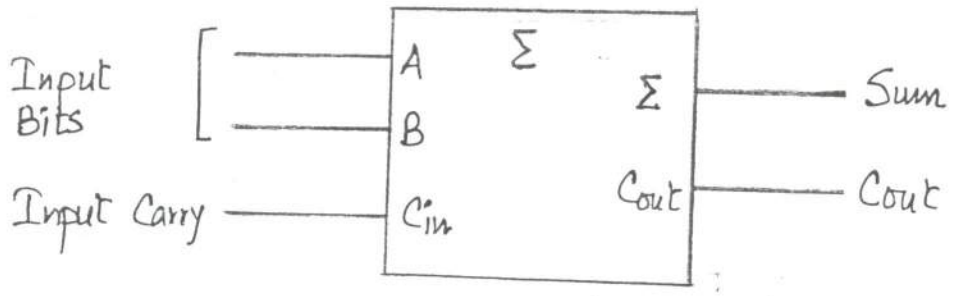


Fig:- Full Adder Logic Symbol.

It consists of three inputs and two outputs. The 2 input variables denoted by A and B represent the two significant bits to be added. The third input, Cin, represents the carry from the previous lower significantposition The outputs are designated by the symbols S (for sum) and Cout (for carry). The truth table for full adder is shown as below:-

Full Adder Truth Table.

A	B	Cin	Σ	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

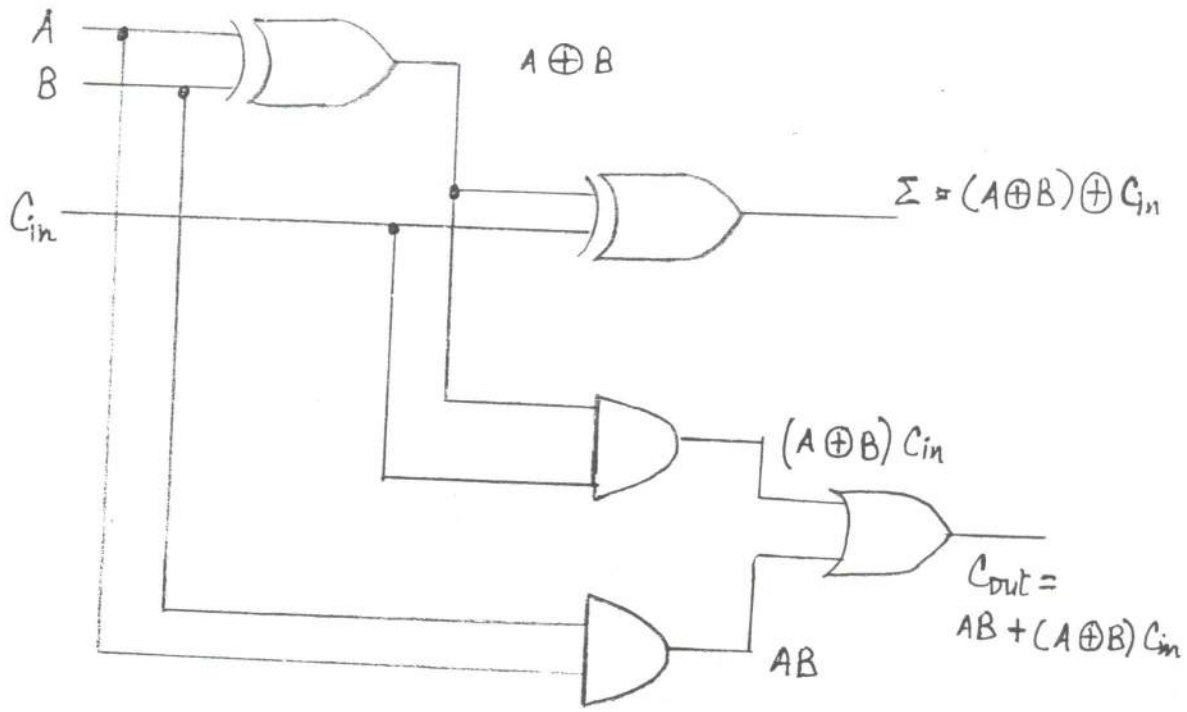
From the truth table, the logic expression for S can be written by summing up the input combinations for which the sum output is 1 as :-

$$S = (A \oplus B) \oplus C_{in} \quad \text{---------- (4)}$$

Similarly, the logic expression for C_{out} can be written by summing up the input combinations for which C_{out} is 1, as given below:-

$$\boxed{C_{out} = AB + (A \oplus B) C_{in}} \quad \text{---- (5)}$$

A full adder circuit using EX-OR Gate implementation is shown as :-



OR

Ans 4 (d) (i) $(657)_8 = (\ ?\ )_{16}$

So, we have to convert an Octal representation of a number into hexadecimal representation.

Steps :-

1. Convert the given number in octal to its binary equivalent.
2. Form groups of 4 bits, starting from LSB.
3. Write the equivalent hexadecimal number for each group of 4 bits.

$(657)_8 = 6 \quad 5 \quad 7$

$= (1\,10\ \ 10\,1\ \ 111)_2$

$\boxed{(657)_8 = (1AF)_{16}}$ Ans.

(ii) $(1D53)_{16} = (\ ?)_{10}$

In this case, we have to convert hexadecimal representation of number into decimal equivalent.

Procedure :-

The conversion from a hexadecimal to a decimal number can be carried out by multiplying each significant digit of the hexadecimal by its respective weight and adding the products.

$(1D53)_{16} = 1 \times 16^3 + D \times 16^2 + 5 \times 16^1 + 3 \times 16^0$

$= 4096 + 13 \times 256 + 80 + 3$

$\boxed{(1D53)_{16} = (7507)_{10}}$ Ans.

(iii) $(131.F2)_{16} = (?)_{10}$

In this case also, we have to convert hexadecimal numbe to decimal number as already done previously in case(ii); so, the procedure is same.

$$(131.F2)_{16} = 1\times16^2 + 3\times16^1 + 1\times16^0 \cdot F\times16^{-1} + 2\times16^{-2}$$

$$= 256 + 48 + 1 + .9375 + \left(\frac{2}{256}\right)$$

$$\boxed{(131.F2)_{16} = (305.945)_{10}}$$ Ans.

Ans 5 (a):- Out of the three transistor connections, the Common Emitter Configuration is widely used because of the following reasons:-

(1) High Current Gain:- The collector current in common Emitter configuration is given by:-

$$I_c = \beta I_B + I_{CEO}$$

Where, I_c = Output current

I_B = Input current

β = Base Current Amplification factor.

As the value of β is very large, therefore, the output current is much more than the input current. Hence, the current gain in common Emitter configuration is very high.

(2) High voltage and power gain:- Due to high current gain, the common emitter configuration has highest voltage and power gain among three transistor configurations.

(3) Moderate output to input Impedance Ratio:- This makes common emitter configuration an ideal one for coupling between various transistor stages.

Ans 5 (b):- Silicon is usually preferred over germanium for fabrication of semiconductor devices because:-

1. Silicon has much higher thermal conductivity; its thermal resistance is, therefore less.
2. Silicon thyristors suffer from low losses; Low temperature rise, and thus more operating life
3. Breakdown voltage is much higher than that of Germanium.
4. Silicon is much cheaper than Germanium.

Ans 5 (c):- Zener Diode:-

When the reverse voltage reaches breakdown voltage in normal PN junction diode, the current through the junction and the power dissipated at the junction will be high. Such an operation is destructive and the diode gets damaged. Whereas diodes can be designed with adequate power dissipation capabilities to operate in the breakdown region. One such a diode is known as Zener diode. Zener diode is heavily doped than the ordinary diode.

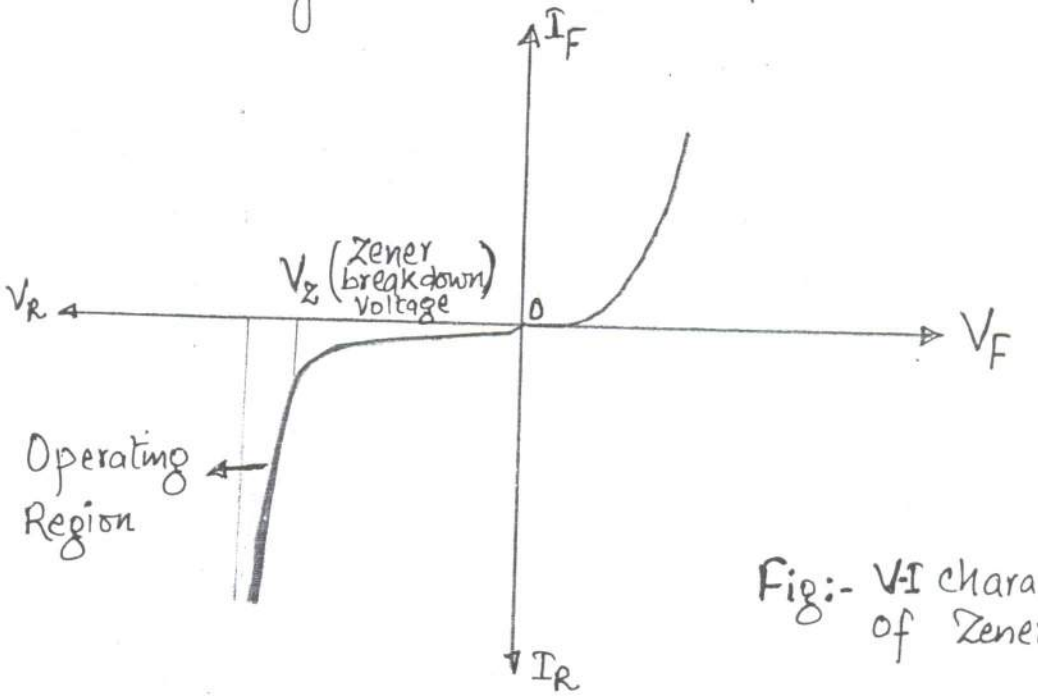


Fig:- V-I characteristics of Zener diode.

From the V-I characteristics of Zener diode shown above, it is found that the operation of Zener diode is same as that of ordinary PN diode under forward-biased condition. Whereas under reverse biased condition, breakdown of the junction occurs. The breakdown voltage depends upon the amount of doping. Since the Zener diode is heavily doped, depletion layer will be thin and, consequently, breakdown occurs at lower reverse voltage and further, the breakdown voltage is sharp.

Applications :-

From the Zener diode characteristics shown above; it is seen that under the reverse bias condition, the voltage across the diode remains almost constant although the current through the diode increases as shown in region AB. Thus, the voltage across the Zener diode serves as a reference voltage. Hence, the Zener diode can be used as a voltage regulator.

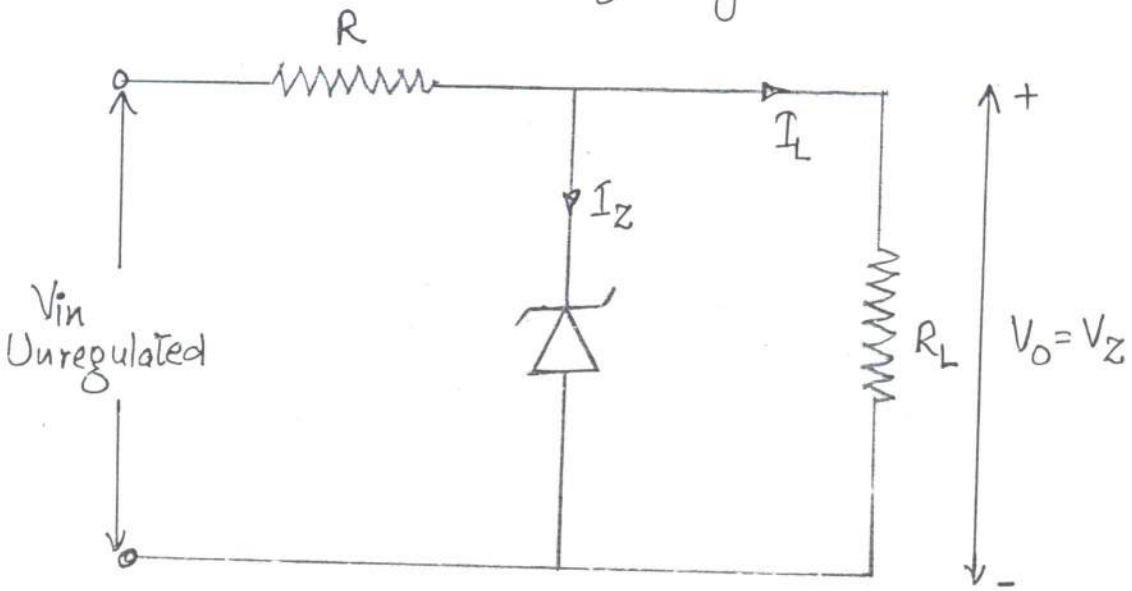


Fig:- Zener Diode as Shunt Regulator.

Ans 5 (d):-

→ Avalanche Multiplication :-

As theapplied reverse bias increases in the PN junction diode, the field across the junction increases correspondingly. Thermally generated carriers while traversing the junction acquire a large amount of kinetic energy from this field. As a result, the velocity of these carriers increases. These electrons disrupt covalent bond by colliding with immobile ions and create new electron-hole pairs. These new carriers again acquire sufficient energy from the field and collide with other immobile ions thereby generating further-

electron hole pairs. This process is cummulative in nature and results in generation of avalanche of charge carriers within a short time. This mechanism of carrier generation is known as **Avalanche Multiplication**. This process results in flow of large amount of current at the same value of reverse bias.

→ Zener Breakdown:-

When the P and N regions are heavily doped, direct rupture of covalent bonds taken place because of the strong electric fields at the junction of PN diode. The new electron-hole pairs so created increase the reverse current in a reverse biased PN junction or diode. The increase in current takes place at a constant value of reverse bias typically below 6V for heavily doped diodes. As a result of heavy doping of P and N regions, the depletion region width becomes very small and for an applied voltage of 6V or less, the field across the depletion region becomes very high, of the order of 10^7 V/m, making conditions suitable for **Zener Breakdown**.

For lightly doped diodes, Zener breakdown voltage becomes high and breakdown is then predominantly by Avalanche multiplication. Though Zener breakdown occurs for lower breakdown voltage and Avalanche breakdown occurs for higher breakdown voltage, such diodes are normally called Zener diodes.

OR

Ans 5(d): Clippers:-

The circuit with which the waveform is shaped by removing (or clipping) a portion of the input signal

without distorting the remaining part of the alternating waveform is called a clipper. Clippers are also referred to as voltage (or current) limiters, amplitude selectors, or slicers. These circuits find extensive use in radars; digital computers; radio and television receivers etc. Clippers are classified into following broad categories:-

a. Positive Clipper.
b. Negative Clipper.
c. Biased Clipper.
d. Combination Clipper.

Positive Clipper:- A positive clipper is that which removes the positive half cycles of the input voltage. A typical positive clipper circuit is shown as follows:-

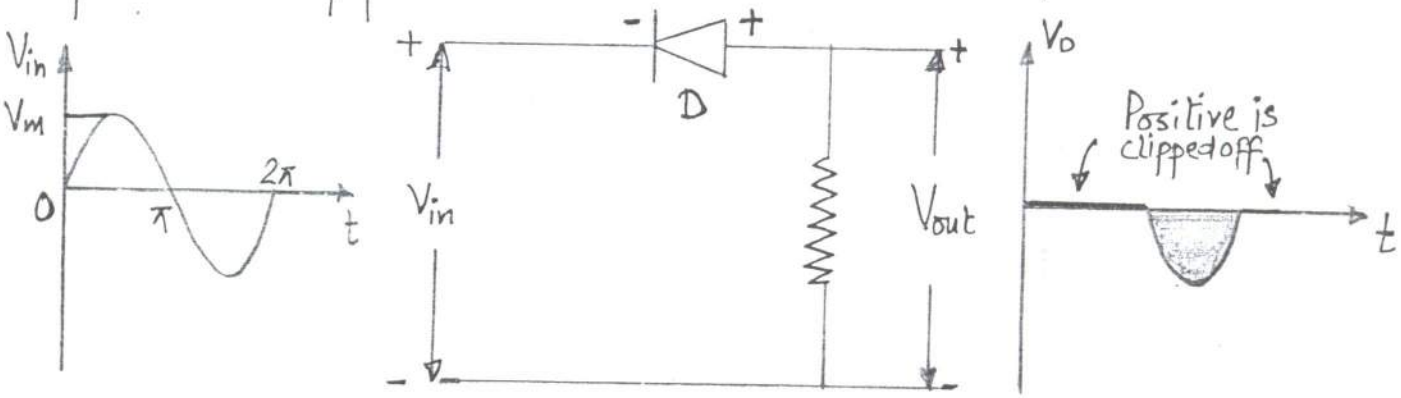


Fig:- Positive Series Clipper.

During the positive half cycle of input voltage, the diode conducts and acts as short circuit and hence there is zero signal at output ie. the positive half cycle is clipped off. When the input signal is negative, the diode does not conduct and acts as an open switch.

Thus the positive clipper has clipped the positive half cycle completely and allowed to pass the negative half cycle of the input signal.

Clampers :- Clamping circuits shifts (clamps) a signal to a different dc level ie. it introduces a dc level to an ac signal. Hence, the clamping network is also known as dc restorer. The key idea behind clamping circuit is shown as follows :-

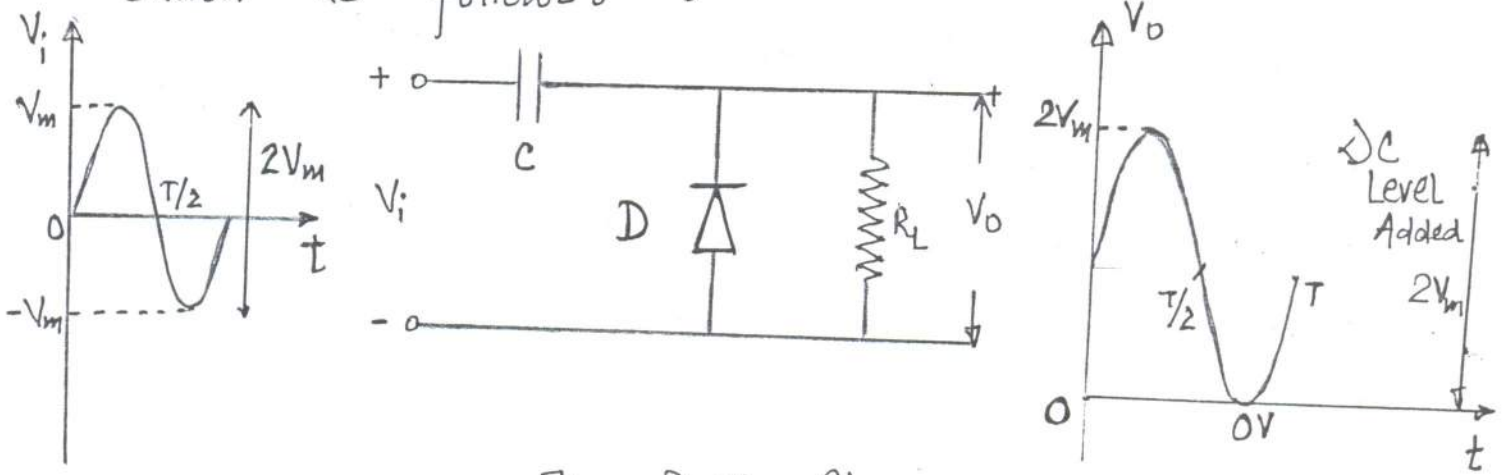


Fig:- Positive Clamper.

The input signal is a sine wave having a peak-to-peak value of 10V. The clamper adds the dc component and pushes the signal upwards so that the negative peaks falls on the zero level.

It may be seen that the shape of the original signal has not changed ; only there is a vertical shift in the signal. Such a clamper is called as Positive Clamper. Clamper circuits find application in television receivers to restore the dc reference signal to video signal.

PN junction as a Rectifier :-

The rectifying action of a pn junction is explained with the help of following circuit diagram :-

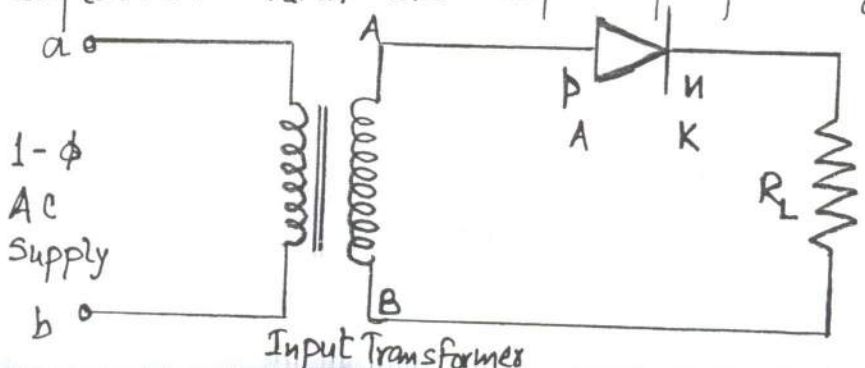


Fig:- Rectifying property of Rectifier.

The ac input voltage to be rectified, the diode and Load R_L are connected in series. The dc output is obtained across the load. During the positive half cycle of ac input voltage, the arrowhead becomes positive with respect to bar or p- becomes positive with respect to n. So, diode is forward biased and conducts current in the circuit. The result is that positive half cycle of input voltage appears across R_L as shown. However, during the negative half cycle of input ac voltage, the diode becomes reverse biased. So, diode does not conduct and no voltage appears across load R_L. In this way pn junction or crystal diode has been able to do rectification i.e. change ac into dc. It may be seen that output across R_L is pulsating dc.